Listing of Claims:

Claim 1 (previously presented): A computer system, comprising:

a processor for performing geometric calculations on a plurality of vertices of a primitive;

a rasterization circuit coupled to the processor that rasterizes the primitive according to a scan conversion process which operates using a floating point format; and

a frame buffer coupled to the rasterization circuit for storing a plurality of color values in the floating point format.

Claim 2 (canceled)

Claim 3 (previously presented): The computer system of Claim 1 further comprising:

a texture circuit coupled to the rasterization circuit that applies a texture to the primitive, wherein the texture is specified by floating point values; and

a texture memory coupled to the texture circuit that stores a plurality of textures in floating point values.

Claim 4 (previously canceled)

Claim 5 (previously presented): The computer system of Claim 1, wherein the floating point format is comprised of sixteen bits.

Claim 6 (original): The computer system of Claim 5, wherein the floating point format is comprised of an slOe5 format.

Claim 7 (previously presented): The computer system of Claim 1 further comprising a lighting circuit coupled to the rasterization circuit for performing a lighting function, wherein the lighting function executes on floating point values.

Claim 8 (previously presented): The computer system of Claim 1 further comprising a fog circuit coupled to the rasterization circuit for performing a fog function, wherein the fog function operates on floating point values.

Claim 9 (previously presented): The computer system of Claim 1 further comprising an antialiasing circuit coupled to the rasterization circuit which performs an antialiasing algorithm according to floating point values.

Claim 10 (previously presented): The computer system of Claim 1 further comprising a blender coupled to the rasterization circuit which blends floating point values.

Claim 11 (previously presented): The computer system of Claim 1 further comprising logic coupled to the rasterization circuit which performs per-fragment operations on floating point values.

Claim 12 (original): The computer system of Claim 1, wherein the processor, the rasterization circuit, and the frame buffer are on a single semiconductor chip.

Claim 13 (original): The computer system of Claim 12, wherein the processor, the rasterization circuit, and the frame buffer reside on a same substrate of the single semiconductor chip.

Claims 14-21 (canceled)

Claim 22 (previously presented): In a computer system, a method for operating on data stored in a frame buffer, comprised of:

a) scan converting the data in a floating point format to produce floating point scan converted data;

b) storing the floating point scan converted data in the frame buffer in the floating point format;

c) reading the floating point scan converted data from the frame buffer;

d) operating directly on the floating point scan converted data in the floating point format to produce color data in the floating point format; and

e) writing the floating point color data to the frame buffer in the floating point format.

Claims 23-25 (canceled)

Claim 26 (previously presented): The method of Claim 22, wherein the steps of writing, storing, and reading are further comprised of specifying the floating point format according to a specification, wherein the specification corresponds to a level of range and precision.

Claim 27 (original): The method of Claim 26 wherein the specification is comprised of 16 bits of data and the data are comprised of one sign bit, ten mantissa bits, and five exponent bits.

Claim 28 (original): The method of Claim 26 wherein the specification is comprised of 17 bits of data and the data are comprised of one sign bit, 11 mantissa bits, and five exponent bits.

Claim 29 (previously presented): The method of Claim 26 wherein the specification is comprised of 16 bits of data and the data are comprised of ten mantissa bits and six exponent bits.

Claim 30 (original): The method of Claim 26 wherein the specification is comprised of 32 bits of data and the data are comprised of one sign bit, 23 mantissa bits, and eight exponent bits.

Claim 31 (previously presented): A computer system comprising:

a raster subsystem for performing a rasterization process, the rasterization process performed in a floating point format; and

a floating point frame buffer coupled to the raster subsystem for storing a plurality of floating point color values, wherein the floating point color values are read out from the frame buffer in the floating point format for display.

Claim 32 (previously presented): The computer system of Claim 31, wherein the floating point color values are written to the frame buffer.

Claim 33 (previously presented): The computer system of Claim 31, wherein the floating point color values are read from the frame buffer for graphics processing.

Claim 34 (canceled)

Claim 35 (previously presented): The computer system of Claim 31, wherein the floating point color values are written to, read from, and stored in the frame buffer using a specification of the floating point color values that corresponds to a level of range and precision.

Claim 36 (original): The computer system of Claim 35, wherein the floating point color values are comprised of 16 bits of data and the data are comprised of one sign bit, ten mantissa bits, and five exponent bits.

Claim 37 (original): The computer system of Claim 35, wherein the floating point color values are comprised of 17 bits of data and the data are comprised of one sign bit, 11 mantissa bits, and five exponent bits.

Claims 38-44 (canceled)

Claim 45 (previously presented): A rendering pipeline, comprising:

a processor for performing geometric calculations on a plurality of vertices of a primitive;

a rasterization module coupled to the processor that rasterizes the primitive according to a scan conversion process which operates using a floating point format; and

a frame buffer coupled to the rasterization module for storing a plurality of color values in the floating point format.

Claim 46 (canceled)

Claim 47 (previously presented): The rendering pipeline of Claim 45, further comprising:

a texture module coupled to the rasterization module that applies a texture to the primitive, wherein the texture is specified by floating point values; and

a texture memory coupled to the texture module that stores a plurality of textures in floating point values.

Claim 48 (previously presented): The rendering pipeline of Claim 45, wherein the floating point format is comprised of sixteen bits.

Claim 49 (previously presented): The rendering pipeline of Claim 48, wherein the floating point format is comprised of an s1Oe5 format.

Claim 50 (previously presented): The rendering pipeline of Claim 45, further comprising a lighting module coupled to the rasterization module for performing a lighting function, wherein the lighting function executes on floating point values.

Claim 51 (previously presented): The rendering pipeline of Claim 45, further comprising a fog module coupled to the rasterization module for performing a fog function, wherein the fog function operates on floating point values.

Claim 52 (previously presented): The rendering pipeline of Claim 45, further comprising an antialiasing module coupled to the rasterization module which performs an antialiasing algorithm according to floating point values.

Claim 53 (previously presented): The rendering pipeline of Claim 45, further comprising a blender coupled to the rasterization module which blends floating point values.

Claim 54 (previously presented): The rendering pipeline of Claim 45, further comprising logic coupled to the rasterization module which performs per-fragment operations on floating point values.

Claim 55 (previously presented): The rendering pipeline of Claim 45, wherein the processor, the rasterization module, and the frame buffer are on a single semiconductor chip.

Claim 56 (previously presented): The rendering pipeline of Claim 55, wherein the processor, the rasterization module, and the frame buffer reside on a same substrate of the single semiconductor chip.

Claim 57 (canceled).

Claim 58 (previously presented): The computer system of Claim 1 further comprising:

a display screen coupled to the frame buffer for receiving the plurality of color values read out from the frame buffer in the floating point format and displaying an image according to the plurality of color values.

Claim 59 (previously presented): The computer system of Claim 1 further comprising:

an electrical connector for forwarding floating point color values from the frame buffer to a display screen.

Claim 60 (previously presented): The computer system of Claim 31 wherein the raster subsystem performs a scan conversion process in a floating point format.

Claim 61 (canceled)

Claim 62 (previously presented): The rendering pipeline of Claim 45 further comprising:

a display screen coupled to the frame buffer for receiving the plurality of color values read out from the frame buffer in the floating point format and displaying an image according to the plurality of color values.

Claim 63 (previously presented): The rendering pipeline of Claim 45 further comprising:

an electrical connector for forwarding floating point color values from the frame buffer to a display screen.